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TRANSLATION OF REJECTION REASONS (Primary Examination)

1. Application No.: 091122692
2. Title of the invention: Semiconductor Device Using Shallow Trench Isolation and Method of Fabricating the Same
3. Applicant: Elpida Memory, Inc.
4. Filed: Oct. 1, 2002
5. Decision: This application is rejected on the ground of the stipulation of Article 20, No. 2 of Patent Law

Rejection Reasons:

This application is mainly characterized in that an insulating film (silicon nitride or silicon oxinitride), whose bottom portion is thinner than the side portion for reducing an internal stress of the semiconductor substrate, is formed to cover a shallow trench. Besides, a silicon oxide film can be formed between the insulating film and the substrate.

However, US 6277706 (cited reference 1), published on Aug. 21, 2001 and entitled "Method of Manufacturing Isolation Trenches Using Silicon Nitride Liner," and its Japanese counterpart "特開平11-3936" (cited reference 2), have disclosed the same technical concept as this application. The disclosed technical concept resides in that a LPCVD silicon nitride film is deposited on the liner oxide film within shallow trenches. Then, as shown in Fig. 2(b) and 2(c), the silicon nitride film in the sidewall of shallow trenches is kept after etching. Furthermore, cited reference 1 has disclosed, in Column 4, Line 56~58 in its specification, that the silicon nitride film after etching is able to reduce stresses to be exerted on the silicon nitride film. Although this application is somewhat different from the above citations regarding whether the bottom of silicon nitride film in the shallow trench or the liner oxide film is provided, the change in the residue thickness after dielectric etching can be easily accomplished for those skilled in the art by controlling the duration of etch time. In addition, as claimed in this application, the change regarding whether there is provided a liner oxide film in the shallow trench depending on the need is obvious to those skilled in the art. It has also been disclosed by TW336344 (cited reference 3), published on Jul. 11, 1998 and entitled "Trench Isolation Region and Method of Fabricating the Same", and particularly in the paragraph from the last line in page 6 to the second line in page 7, and also the paragraph of Line 7~9 in Page 7

in the specification of TW336344. Consequently, this application lacks inventive step.

Summing up the above, this application utilizes technology in existence prior to its filing date, and can be easily achieved by a person having ordinary skill in the art. This application does not meet the statutory requirements for patentability, and thus should not be granted a patent according to the stipulation of Article 20, No. 2 of Patent Law.

TRENCH ISOLATION AND METHOD FOR FORMING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention:

The invention relates to a method for forming an isolation in integrated circuit processes and, more particularly, to a method for improving the quality of a trench isolation so as to control the area of the isolation.

Description of the Related Art:

In the manufacturing process of an integrated circuit, the isolation formed between devices plays a very important role. Generally, when manufacturing an integrated circuit, an isolation must be formed before forming devices. When performing subsequent processes, in a large scale integrated circuit or very large scale integrated circuit, a small leak current from each device circuit leads to a significant amount of energy dissipation of the whole circuit. Therefore, forming an effective isolation between devices is very important for forming the integrated circuit. In addition, the design of the integrated circuit tends to minimize sizes of devices and maximize the packing density of a wafer. Therefore, it becomes more difficult to form effective isolations in a smaller area, and it is challenging to form effective isolations in the field of sub-micron technology.

There are several kinds of processes being used to form isolations

in integrated circuits, for example, local oxidation of silicon (LOCOS) and shallow trench isolation (STI). LOCOS is an isolation technique being extensively used in semiconductor processes, by which a mask is formed on a semiconductor silicon wafer by lithography to expose a portion of the silicon wafer, and then the mask is used in an oxidation process to oxidize the exposed portion into an insulating area of silicon dioxide on the surface of the silicon wafer, which is often called field oxides (FOX). This isolation process can provide an effective insulation. However, when the sizes of devices are reduced, this LOCOS process reaches its limit. For example, the bird's beak of the field oxide will go into the active area of the devices, which reduces a usable area and thus is a disadvantage for forming the devices. Since the topography of the LOCOS that protrudes on the wafer surface is unfavorable in device miniaturization for sub-micron process, a trench isolation technique is increasingly used for forming the isolation between active regions.

For the above reasons, the trench isolation technique is widely used in VLSI and ULSI technology for forming the insulation region between devices. Therefore, the trench isolation technique can be used to replace the conventional LOCOS process. The trench isolation process first forms silicon nitrides on a wafer as a stop layer for a subsequent planarization process, an etching mask is then formed on the silicon nitrides by lithography, and the etching mask is used to perform an etching process forming a trench in a wafer. Oxides are back-filled into the trench by chemical vapor deposition (CVD), and back-etching or chemical mechanical polishing is used for forming a favorable

topography thereof. ...

However, the quality of oxide layer formed by CVD is not as good as that formed by thermal oxidation, thus the quality of oxides of conventional trench isolation technique is lower than that of the LOCOS. In sub-micron process, insulation quality is very important, hence the conventional trench isolation technique requires an additional thermal process for increasing the density of oxide layer. During this thermal process, a thin oxide layer forms and surrounds the periphery of the trench isolation, which increases the isolation area. Thus the conventional process is unable to control the exact isolation area. Precision in size control is very important in sub-micron process, therefore a method that provides good oxide quality and controls isolation area precisely is needed.

SUMMARY OF THE INVENTION

An object of the invention is to form isolations between integrated circuit devices.

Another object of the invention is to provide a better oxide quality for isolations and to control the isolation areas with precision.

The invention first forms a silicon dioxide layer on a wafer as a pad, then, a trench forms in the wafer, a thin silicon dioxide layer forms on the surface of the trench thereafter, then a silicon nitride layer forms on the pad and along the surface of the trench. This silicon nitride layer is a stop layer for subsequent planarization process, and when subsequently a trench oxide layer is formed by thermal oxidation, the silicon nitride layer

can be used to inhibit the oxide layer from expanding into the wafer, therefore controls the isolation area with precision. A silicon layer then forms on the silicon nitride layer and back-fills into a portion of the trench, then controls the silicon amount in the trench by chemical mechanical polishing or back-etching. The next step is to oxidize silicon by thermal oxidation for forming an isolation oxide layer in the trench; the quality of oxide layer formed by thermal oxidation is better than that formed by conventional CVD, also, the silicon nitride layer formed around the trench surface inhibits the oxide layer from expanding into the wafer thus controls the area of the oxide layer. Afterwards, dry etching is utilized to remove the silicon nitride layer formed on the wafer surface, then again remove the pad by dry etching, and finally forms the trench isolation as the invention intended. The abovementioned two dry etching processes can select process parameters of lower selectivity for silicon dioxide to silicon nitride, for example 1 to 1, also one can use chemical mechanical polishing process to remove the aforementioned silicon nitride and silicon dioxide.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a sectional view illustrating a pad and a trench in a wafer formed from the invention.

FIG. 2 is a sectional view illustrating a silicon nitride layer in a trench and on a pad formed from the invention.

FIG. 3 is a sectional view illustrating a silicon layer on a silicon nitride layer formed from the invention.

FIG. 4A is a sectional view illustrating planarization process by chemical mechanical polishing in the invention.

FIG. 4B is a sectional view illustrating planarization process by back-etching in the invention.

FIG. 5A is a sectional view illustrating silicon oxide in the trench formed by thermal process corresponding to FIG. 4A in the invention.

FIG. 5B is a sectional view illustrating silicon oxide in the trench formed by thermal process corresponding to FIG. 4B in the invention.

FIG. 6A is a sectional view illustrating the removal of silicon nitride and pad layer using dry etching method in the invention.

FIG. 6B is a sectional view illustrating the removal of silicon nitride and pad layer using chemical mechanical polishing in the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The invention discloses a method for improving the quality of isolation oxides, the disclosed method also can accurately control the isolation area; the invention is further explained below.

Referring to FIG. 1, a thin layer of silicon dioxide acting as a pad layer 4 forms on a P-type or N-type silicon semiconductor wafer 2 with <100> crystal orientation; pad layers are often formed by thermal oxidation, this pad layer 4 has a thickness around 50 – 500 angstrom (Å). A resist pattern is formed on the pad layer 4 for defining a trench isolation area, then the pad layer 4 and wafer 2 are etched with the resist pattern as a mask to form a trench 6 in the wafer 2, the depth of the trench 6 is generally from 2000 to 8000 Å measuring from the surface of the pad

layer 4. The resist pattern is removed after the trench has been made. After making the trench 6, a silicon dioxide layer (not illustrated) that covers the surface of the trench 6 can be formed; this is a nonessential step, and one may choose to omit it. In general, this silicon dioxide layer can be formed by chemical vapor deposition (CVD) or thermal oxidation; in addition, for achieving the aforementioned purpose, the pad layer 4 can be deposited after the formation of the trench 6, so that the silicon dioxide is formed in the trench and on the surface of the wafer at once.

Referring to FIG. 2, a silicon nitride layer 8 with a thickness of 500 to 2000 Å is formed on the pad layer 4 and along the surface of the trench 6, this silicon nitride layer 8 will be used as a stop layer in a subsequent planarization process. Moreover, later in the process, the silicon nitride layer 8 will inhibit an oxide layer from expanding into the wafer 2 where the oxide layer is formed by thermal oxidation, thus the invention can control the exactness of width and length of the isolation. As well, one can substitute the aforementioned silicon nitride with silicon oxynitride. In a preferred embodiment, the silicon nitride layer 8 is formed by either low pressure chemical vapor deposition (LPCVD), plasma enhance chemical vapor deposition (PECVD), or high density plasma chemical vapor deposition (HDPCVD); process temperature is around 350 – 800 degrees Celsius (℃) (350 – 450℃ for PECVD, 700 – 800℃ for LPCVD), the reaction gas are SiH_4, NH_3, N_2, N_2O or SiH_2Cl_2, NH_3, N_2, N_2O.

Referring to FIG. 3, a silicon layer 10 is formed on the

abovementioned silicon nitride layer 8, the silicon layer 10 also back-fills into portion of the trench 6 and deposits along the surface of the trench 6, for a preferred embodiment, the silicon layer 10 is of polysilicon or amorphous silicon formed by CVD, wherein the thickness of silicon layer 10 varies according to the dimension of the trench 6 and the amount of silicon required to oxidize.

Referring to FIG. 4A and FIG. 4B, chemical mechanical polishing and back-etching can be used to remove the silicon layer 10 outside of the trench. For a preferred embodiment, chemical mechanical polishing is more favorable. As shown in FIG. 4A, there are more silicon layer 10 remaining in the trench 6 which is beneficial in forming isolation oxide layer by thermal oxidation thereafter, whereas back-etching process stops etching at the surface of the silicon nitride layer 8 with silicon layer 10 remaining on the sidewalls of the trench 6 as shown in FIG. 4B.

Referring to FIG. 5A and FIG. 5B, the next step is to oxidize the silicon layer 10 using thermal oxidation for forming an isolation oxide layer 12 in the trench 6; the remaining silicon layer 10 in the trench 6 will go through thermal oxidation and transform into silicon dioxide 12 in the trench as an insulating substance. FIG. 5A and FIG. 5B are sectional views of FIG. 4A and FIG. 4B after oxidation, respectively; the reaction temperature and oxidation time of the oxidation process varies with the amount of silicon available. The quality of oxide layer 12 made by thermal oxidation is better than that made by conventional CVD method. Furthermore, the silicon nitride layer 10 is formed on and around all surfaces of the trench 6, therefore when the oxide layer 12 is formed by

thermal oxidation, the oxide layer 12 is unable to expand into the wafer 2 because the silicon nitride layer acts as a barrier; thus the area of oxide layer 12 can be controlled with precision. This method effectively controls the area of isolation in sub-micron process, hence is advantageous in device miniaturizations.

Referring to FIG. 6A, the next step is to remove the silicon nitride layer 8 formed on the wafer 2 by dry etching. This step can utilize CF_4, CHF_3, C_2F_6 or C_3F_8 for performing plasma etching, and then use dry etching to remove the pad layer 4. In the process of removing pad layer, partial of the isolation oxide layer 12 is removed as well; the final structure is the trench isolation of the invention. The two aforementioned dry etching processes can select process parameters of lower selectivity for silicon dioxide to silicon nitride, and the two processes can be done in the same machine to save process time and cost; or one can use chemical mechanical polishing method instead, the structure resulted therefrom is shown in FIG. 6B.

Some advantages of the invention are the prevention of the oxide layer formation around the trench for controlling isolation area and higher oxide quality for insulation.

Please note that some elements in the invention can be substituted with other elements that would give similar results. For example, one can substitute the silicon nitride layer with a silicon oxynitride layer; the planarization process can utilize either chemical mechanical polishing or dry etching.

While the invention has been described by way of example and in

terms of the preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

1. A method for forming a trench isolation in a semiconductor wafer, comprising the steps of:

forming a trench in the wafer;

forming a silicon-containing nitrite layer on the wafer and along a surface of the trench;

providing a predetermined amount of silicon in the trench;

performing a thermal process to form an silicon oxide layer oxidized from the predetermined amount of silicon as an insulating substance of the trench isolation; and

removing the silicon-containing nitrite layer formed on the wafer.

2. The method as in claim 1, further comprising the following steps for forming the trench:

forming a photoresist on the wafer to define an area for the trench;

etching the wafer by using the photoresist as a mask; and

removing the photoresist.

3.The method as in claim 1, wherein an oxide pad layer is formed on the wafer before forming the trench.

4. The method as in claim 3, further comprising the step of:

removing the oxide pad layer after removing the silicon-

containing nitrite layer.

5. The method as in claim 4, wherein the oxide pad layer is formed of silicon oxide.

6. The method as in claim 5, wherein the oxide pad layer is removed by dry etching using a plasma containing carbon fluoride.

7. The method as in claim 5, wherein the oxide pad layer is removed by chemical mechanical polishing.

8. The method as in claim 5, wherein the oxide pad layer has a thickness of about 50 to 500 Å.

9. The method as in claim 1, further comprising forming the predetermined amount of silicon on the wafer when providing the predetermined amount of silicon in the trench.

10. The method as in claim 9, further comprising removing the predetermined amount of silicon formed on the wafer by chemical mechanical polishing after providing the predetermined amount of silicon in the trench.

11. The method as in claim 9, further comprising removing the

predetermined amount of silicon formed on the wafer by dry etching after providing the predetermined amount of silicon in the trench.

12. The method as in claim 1, wherein the silicon-containing nitrite layer has a thickness of about 500 to 2000 Å.

13. The method as in claim 1, wherein the silicon-containing nitrite layer is a silicon oxynitride layer.

14. The method as in claim 1, wherein the silicon-containing nitrite layer is a silicon nitride layer.

15. The method as in claim 1 or 5, wherein the silicon-containing nitrite layer is removed by dry etching using a plasma containing carbon fluoride.

16. The method as in claim 1 or 5, wherein the silicon-containing nitrite layer is removed by chemical mechanical polishing.

17. The method as in claim 1, wherein the predetermined amount of silicon is formed of polysilicon.

18. The method as in claim 1, wherein the predetermined amount of silicon is formed of amorphous silicon.

19. The method as in claim 1, wherein the silicon-containing nitrite layer is formed by low pressure chemical vapor deposition (LPCVD), plasma enhance chemical vapor deposition (PECVD), or high density plasma chemical vapor deposition (HDPCVD).

20. The method as in claim 19, wherein the reaction gas is SiH_4, NH3, N_2 and N_2O.

21. The method as in claim 19, wherein the reaction gas is SiH_2Cl_2, NH3, N_2 and N_2O.

22. The method as in claim 1, wherein the thermal process is performed in an oxygen-containing environment.

Abstract

A method for forming a trench isolation utilizes a silicon nitride layer to accurately control the area of trench isolation, and utilizes thermal oxidation to improve the quality of insulating substance for the trench. The method first forms a silicon nitride layer on the trench surface of a wafer, then deposits a silicon layer which back fills into the trench, performs a planarization process which flattens the silicon layer surface, next performs an oxidation process to oxidize the silicon layer into a silicon oxide layer, and finally removes the silicon nitride layer on the wafer.

中 華 民 國 專 利 公 報 (19)(12)

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(三)

(54)名稱：溝渠式隔離區以及其形成之方法

(21)申請案號：86105686

(22)申請日期：中華民國86年(1997)04月29日

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[57]申請專利範圍：

1.一種形成溝渠式隔離區於半導體晶圓中之方法，該方法至少包含：
形成一溝渠於該晶圓之中；
形成一含氮矽化物層於該晶圓之上以及沿著該溝渠之表面沈積；
在該溝渠之中提供預定量之矽；
施以熱處理製程將該預定量之矽氧化形成氧化矽層做為該溝渠式隔離區之絕緣物質；及
去除形成於該晶圓上之該含氮矽化物層。

2.如申請專利範圍第1項之方法，更包含下列步驟以形成該溝渠：
形成一光阻於該晶圓之上以定義該溝渠之區域；
以該光阻為蝕刻罩幕蝕刻該晶圓；及
去除該光阻。

3.如申請專利範圍第1項之方法，其中形成該溝渠之前更包含形成氧化墊層於該晶圓之上。

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4.如申請專利範圍第3項之方法，其中去除該含氮矽化物層之後更包含去除該氧化墊層。

5.如申請專利範圍第4項之方法，其中上述之氧化墊層為氧化矽組成。

6.如申請專利範圍第5項之方法，其中形成上述之氧化墊層為利用含有氟化碳之電漿以乾蝕刻方式去除。

7.如申請專利範圍第5項之方法，其中形成上述之氧化墊層為利用化學機械研磨方式去除。

8.如申請專利範圍第5項之方法，其中上述之氧化墊層之厚度約為50至500埃。

9.如申請專利範圍第1項之方法，其中提供上述預定量之矽於該溝渠中時更包含形成上述預定量之矽於該晶圓之上。

10.如申請專利範圍第9項之方法，其中提供上述預定量之矽於該溝渠中之後更包含施以化學機械研磨方式去除形成於該晶圓上之上述預定量之矽。

公告本

申請日期	86、4、29
案號	86105687
類別	H01L 21/76

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（以上各欄由本局填註）

發明 ~~新型~~ 專利說明書

一、發明 ~~新型~~ 名稱	中文	溝渠式隔離區以及其形成之方法
	英文	
二、發明 ~~創作~~ 人	姓名	林大器
	國籍	中華民國
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三、申請人	姓名（名稱）	台灣積體電路製造股份有限公司
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	代表人姓名	張忠謀

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四、中文發明摘要（發明之名稱：　　）

溝渠式隔離區以及其形成之方法

本發明利用一氮化矽層準確地控制溝渠式隔離區之範圍以及利用熱氧化製程形成之氧化層提昇溝渠填充物之品質，本發明首先形成氮化矽層於晶圓中之溝渠表面，接著再沈積一矽層回填進入溝渠之中，利用平坦化製程將矽層表面平坦化，然後施以氧化製程將矽層氧化成氧化矽層，最後去除形成於晶圓上之氮化矽層。

英文發明摘要（發明之名稱：　　）

（請先閱讀背面之注意事項再填寫本頁各欄）

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訂

線

五、發明說明（　）

發明領域：

本發明與一種積體電路製程中隔離區之形成方法有關，特別是一種增進溝渠式隔離區品質以及控制隔離區範圍之方法。

發明背景：

在積體電路之製造過程中，形成在元件間做爲絕緣之隔離區域扮演著十分重要之角色，一般在製造積體電路時，必須在形成元件之前將隔離區製作完畢，在進行後續之製程，在大型積體電路或是超大型積體電路中，每個元件的微小漏電流都將會造成整個電路中可觀之能量散失。因此，製作元件間有效的隔離區域對於積體電路製程而言非常重要。此外，積體電路之設計傾向於將元件縮小以及提高晶圓之裝構密度(packing density)，所以在更小之區域內製作有效的隔離區益形困難，並且在次微米技術中製作有效之隔離區是一項具挑戰性之工作。

目前正有數種不同製作隔離區之技術應用於積體電路之製程，例如矽區域氧化製程(local oxidation of silicon；LOCOS)、淺溝渠式隔離區製程(shallow trench isolation; STI)等。LOCOS製程爲一種被廣泛應用於半導體製程中的一種隔離技術，其製程主要是在半導體矽晶圓

五、發明說明（　）

上利用微影製程形成一罩幕且曝露出部份之矽晶圓，接著利用該罩幕進行氧化製程將被曝露之區域氧化形成隆起於矽晶圓表面之二氧化矽之絕緣區域，通常稱做場氧化層(field oxides; FOX)，此種隔離製程能夠提供有效地絕緣阻隔。但是當元件之尺寸逐漸縮小化時，傳統之LOCOS製程將會達到一個應用上與製程上的極限，例如場氧化層之鳥嘴效應(bird's beak)將深入元件之主動區域內，在元件可利用空間減小之下，此種現象對元件製程而言是一項不利之因素，另外是對次微米之製程而言LOCOS凸起於晶圓表面，其外觀之地形地勢(topography)不佳不利於元件之縮小，因此利用溝渠式隔離區技術來製作主動區域間之絕緣區域逐漸受到重視。

由於上述之因素，所以在VLSI與ULSI技術中大量採用溝渠式隔離區技術(trench isolation)形成絕緣區域做爲元件間之絕緣區域，因此，此技術能夠用來將取代傳統之LOCOS製程。溝渠式隔離區製程首先形成氮化矽於晶圓之上做爲後續平坦化製程之停止層，然後利用微影技術形成一蝕刻罩幕於氮化矽之上，然後利用該蝕刻罩幕施以蝕刻製程形成溝渠於晶圓之中，以化學氣相沈積(CVD；chemical vapor deposition)之氧化層回填進入溝渠中，接著再利用回蝕刻或是化學機械研磨法將氧化層子以平坦化以得到較佳之外觀地勢(topography)。

五、發明說明（　）

但是以化學氣相沈積法所形成之氧化層之品質較以熱氧化法所形成者爲差，因此習知溝渠式隔離技術之絶緣區氧化物之品質略遜於以LOCOS方法所形成者，而在次微米製程中，絶緣之品質益形重要，因此習知溝渠式隔離技術需要額外之熱處理製程來增進氧化層之緻密性，在此熱處理製程亦會同時形成薄之氧化層環繞於溝渠隔離區之表面，而擴增隔離區之區域，因此傳統之製程將無法精確控制溝渠式隔離區之範圍，但是精確控制尺寸在次微米製程中十分重要，因此目前需要一種不但能夠提供好的氧化層品質而且可以準確控制隔離區域尺寸之方法。

發明目的及概述：

本發明之目的爲一種積體電路中元件間隔離區之製程。

本發明之另一目的爲提供一種具有較佳氧化層品質之隔離區製程以及準確控制隔離區範圍之製程。

本發明可先形成二氧化矽層於一晶圓之上做爲墊層，接著，一溝渠形成於晶圓之中，形成溝渠之後可以先形成一薄的二氧化矽層於溝渠之表面，然後一氮化矽層形成於該墊層之上以及沿著溝渠之表面沈積，此氮化矽層做爲後續平坦化製程之停止層(stop layer)，並且氮化矽層將可以在後續以熱氧化形成溝渠氧化層時抑制氧化層之

五、發明說明（　）

擴張至晶圓之中，因此可以準確地控制隔離區之範圍。一矽層接著形成於上述之氮化矽層之上並回填進入部份之溝渠之中，接著對矽層施以化學機械研磨或是回蝕刻來控制溝渠內的矽量，下一步驟爲施以熱氧化法將矽氧化以形成隔離氧化層於溝渠之中，利用熱氧化製程之氧化層品質較傳統方法使用CVD形成之氧化層優良，另外，氮化矽層環繞形成於溝渠之四周表面將可以阻止氧化層向外擴張進入晶圓之中而準確地控制氧化層之範圍。隨後，利用乾蝕刻去除形成於晶圓表面上之氮化矽層，接著再藉由乾蝕刻去除墊層，最後得到本發明之溝渠式隔離區，上述兩次乾蝕刻製程可以採用對二氧化矽與氮化矽之蝕刻選擇性較低之製程參數(例如1比1)，亦可以使用化學機械研磨製程來去除上述之氮化矽層以及二氧化矽層。

圖式簡單說明：

第一圖爲本發明製程中形成墊層以及溝渠於晶圓中之截面圖。

第二圖爲本發明製程中形成氮化矽層於溝渠中以及墊層上之截面圖。

第三圖爲本發明製程中形成矽層於氮化矽層上之截面圖。

第四圖A爲本發明製程中施以化學機械研磨平坦化製程之截面圖。

五、發明說明（　）

第四圖B爲本發明製程中施以回蝕刻平坦化製程之截面圖。

第五圖A爲本發明製程中相對應於第四圖A施以熱處理製程形成氧化矽於溝渠中之截面圖。

第五圖B爲本發明製程中相對應於第四圖A施以熱處理製程形成氧化矽於溝渠中之截面圖。

第六圖A爲本發明製程中以乾蝕刻方式去除氮化矽以及墊層之截面圖。

第六圖B爲本發明製程中以化學機械研磨方式去除氮化矽以及墊層之截面圖。

發明詳細說明：

本發明揭示一種增進隔離氧化層品質方法，除此之外並可以準確控制隔離區之範圍，本發明將詳細說明如下。

如第一圖所示，一P型或N型具有<100>晶向之矽半導體晶圓2上形成一薄之二氧化矽做爲墊層(pad layer)4，此墊層通常爲利用熱氧化方式形成，此墊層4之厚度約爲50-500埃之間。接著，一光阻圖案形成於墊層4之上用以定義一溝渠式隔離區之區域，然後以此光阻圖案做爲蝕刻罩幕將墊層4以及晶圓2蝕刻形成一溝渠6於晶圓2之中，通常溝渠6之深度由墊層4之表面計算約爲2000至8000埃之間。完成溝渠之後則將上述之光阻圖案去除。在完成溝渠

五、發明說明（　）

6之後可以先形成一二氧化矽層(圖中未示出)覆蓋於溝渠6之表面，此步驟爲非必要之步驟，可以不用實施，一般而言，此二氧化矽層可以採用化學氣相沈積或是熱氧化形成，另外，爲達到上述之目的，墊層4可以在形成溝渠6之後再沈積，如此可以同時形成二氧化矽於溝渠之中與晶圓2之表面。

參閱第二圖，一厚度爲500至2000埃之氮化矽層(silicon nitride)8形成於該墊層4之上以及沿著溝渠6之表面沈積，此氮化矽層8將做爲後續平坦化製程之停止層(stop layer)，另外，氮化矽層8可以在後續製程中以熱氧化形成溝渠氧化層時抑制氧化層之擴張至晶圓2之中，因此本發明可以準確地控制隔離區之寬度與長度，其次，亦可以使用氮氧化矽來取代上述之氮化矽，上述之氮化矽層8以較佳實施例而言可以利用低壓化學氣相沈積法(Low Pressure Chemical Vapor Deposition; LPCVD)、電漿增強式化學氣相沈積法(Plasma Enhance Chemical Vapor Deposition; PECVD)、或高密度電漿化學氣相沈積法(High Density Plasma Chemical Vapor Deposition; HDPCVD)形成，製程溫度爲350-800℃之間(使用PECVD之製程溫度約爲350-450℃，使用LPCVD之製程溫度約爲700-800℃)，反應氣體爲SiH_4, NH_3, N_2, N_2O 或 SiH_2Cl_2, NH_3, N_2, N_2O。

五、發明說明（　）

參閱第三圖，一矽層10接著形成於上述之氮化矽層8之上，矽層10並回填進入部份之溝渠6之中以及沿著溝渠6之表面沈積，以最佳實施例而言，矽層10爲利用化學氣相沈積法形成之複晶矽或是非晶形矽，此製程中矽層10之厚度視溝渠6之大小及所需氧化之矽量而改變。

參閱第四圖A與第四圖B，將溝渠以外之之矽層10除去，可以採用化學機械研磨法或是回蝕刻法來追行，以最佳實施例而言，而以使用化學機械研磨法爲佳，其結果如第四圖A所示，在溝渠6中有較多之矽層10殘留利於後續之熱氧化製程形成隔離氧化層，另外，利用回蝕刻製程之結果如第四圖B所示，蝕刻將停止於氮化矽層10之表面，在溝渠6之側壁將有矽層10殘留。

參閱第五圖A與第五圖B，下一步驟爲以熱氧化法將矽層10氧化以形成隔離氧化層12於溝渠6之中，殘存於溝渠6中矽層將因熱氧化製程之實施而轉變爲二氧化矽12形成於溝渠6之中做爲絕緣之填充物質，第五圖A與第五圖B分別代表相對應於第四圖A與第四圖B經過氧化後之截面圖，此氧化製程之反應溫度與氧化時間端視矽量而改變，利用熱氧化製程之氧化層12品質較傳統方法使用CVD形成之氧化層優良，此外，因爲氮化矽層10環繞形成於溝渠6之四周表面，是故以熱氧化形成氧化層12時將因爲氮化矽層10之阻隔使得氧化層12無法向外擴張進入晶圓2之

五、發明說明（　）

中，進而準確地控制隔離氧化層12之範圍，此方法在次微米製程中能夠有效控制隔離區之大小，利於縮小化之發展。

參閱第六圖A，下一步驟爲利用乾蝕刻方式去除形成於晶圓2表面上之氮化矽層8，此步驟可以使用CF_4、CHF_3、C_2F_6或C_3F_8進行電漿蝕刻，接著再使用乾蝕刻去除墊層4，去除墊層過程中部份之隔離氧化層12將被去除，最後結構爲本發明之溝渠式隔離區。前述兩次乾蝕刻可選擇對二氧化矽欲氮化矽蝕刻選擇比較低之製程參數，而可以在同一機台中爲之，以節省製程時間與成本，或者亦可以化學機械研磨方式進行，其所得之結構如第六圖B所示。

本發明之優點爲可以防止氧化層形成於溝渠之四周而準確控制隔離區之範圍，而且隔離區氧化物之品質較緻密具有較優良之絶緣效果。

本發明以較佳實施例說明如上，而熟悉此領域技藝者，在不脫離本發明之精神範圍內，當可作些許更動潤飾，例如，本發明除了可以利用氮化矽層控制隔離區之範圍外，亦可以使用氮氧化矽層代替氮化矽層，其次，本發明之平坦化製程可以使用化學機械研磨法或是回蝕刻法，其專利保護範圍更當視後附之申請專利範圍及其等同

五、發明說明（　　）

領域而定。

（請先閱讀背面之注意事項再填寫本頁）

裝

訂

六、申請專利範圍

1.一種形成溝渠式隔離區於半導體晶圓中之方法，該方法至少包含：

形成一溝渠於該晶圓之中；

形成一含氮矽化物層於該晶圓之上以及沿著該溝渠之表面沈積；

在該溝渠之中提供預定量之矽；

施以熱處理製程將該預定量之矽氧化形成氧化矽層做爲該溝渠式隔離區之絕緣物質；及

去除形成於該晶圓上之該含氮矽化物層。

2.如申請專利範圍第1項之方法，更包含下列步驟以形成該溝渠：

形成一光阻於該晶圓之上以定義該溝渠之區域；

以該光阻爲蝕刻罩幕蝕刻該晶圓；及

去除該光阻。

3.如申請專利範圍第1項之方法，其中形成該溝渠之前更包含形成氧化墊層於該晶圓之上。

4.如申請專利範圍第3項之方法，其中去除該含氮矽化物層之後更包含去除該氧化墊層。

5.如申請專利範圍第4項之方法，其中上述之氧化墊層爲

六、申請專利範圍

氧化矽組成。

6.如申請專利範圍第5項之方法，其中形成上述之氧化墊層爲利用含有氟化碳之電漿以乾蝕刻方式去除。

7.如申請專利範圍第5項之方法，其中形成上述之氧化墊層爲利用化學機械研磨方式去除。

8.如申請專利範圍第5項之方法，其中上述之氧化墊層之厚度約爲50至500埃。

9.如申請專利範圍第1項之方法，其中提供上述預定量之矽於該溝渠中時更包含形成上述預定量之矽於該晶圓之上。

10.如申請專利範圍第9項之方法，其中提供上述預定量之矽於該溝渠中之後更包含施以化學機械研磨方式去除形成於該晶圓上之上述預定量之矽。

11.如申請專利範圍第9項之方法，其中提供上述預定量之矽於該溝渠中之後更包含施以乾蝕刻方式去除形成於該晶圓上之上述預定量之矽。

12.如申請專利範圍第1項之方法，其中上述之含氮矽化物層厚度約爲500至2000埃。

六、申請專利範圍

13.如申請專利範圍第1項之方法，其中上述之含氮矽化物層爲氮氧化矽層。

14.如申請專利範圍第1項之方法，其中上述之含氮矽化物層爲氮化矽層。

15.如申請專利範圍第1或5項之方法，其中上述之氮化矽層爲利用含有氟化碳之電漿以乾蝕刻方式去除。

16.如申請專利範圍第1或5項之方法，其中上述之氮化矽層爲利用化學機械研磨方式去除。

17.如申請專利範圍第1項之方法，其中上述之預定量之矽爲複晶矽組成。

18.如申請專利範圍第1項之方法，其中上述之預定量之矽爲非晶形矽組成。

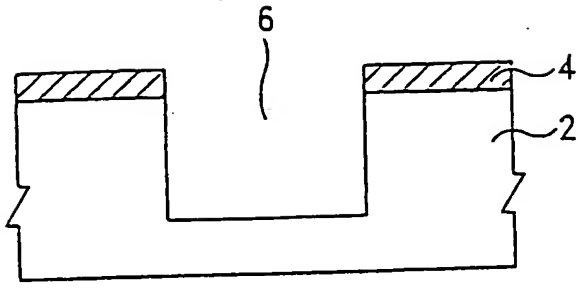
19.如申請專利範圍第1項之方法，其中上述之氮化矽層可以利用低壓化學氣相沈積法(Low Pressure Chemical Vapor Deposition; LPCVD)、電漿增強式化學氣相沈積法(Plasma Enhance Chemical Vapor Deposition; PECVD)以及高密度電漿化學氣相沈積法(High Density Plasma Chemical Vapor Deposition; HDPCVD)形成。

六、申請專利範圍

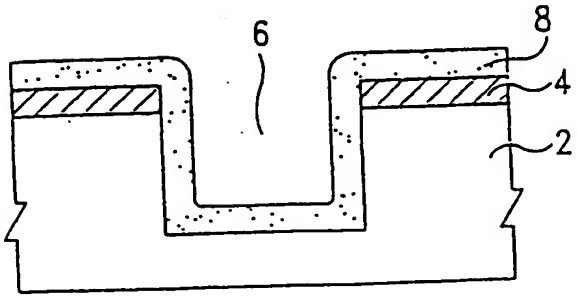
20.如申請專利範圍第19項之方法，其中上述之反應氣體爲SiH_4, NH_3, N_2與N_2O。

21.如申請專利範圍第19項之方法，其中上述之反應氣體爲SiH_2Cl_2, NH_3, N_2與N_2O。

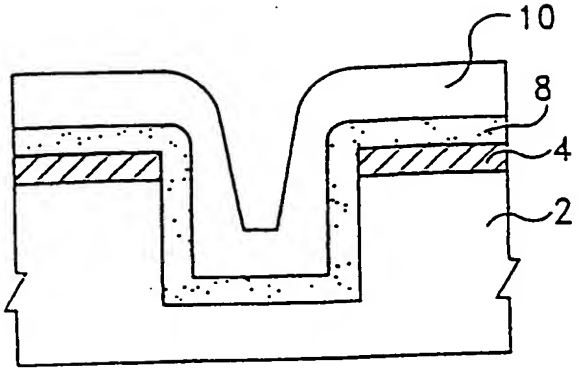
22.如申請專利範圍第1項之方法，其中上述之熱處理製程在含氧環境中進行。



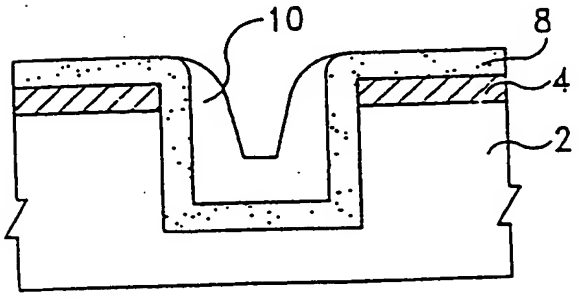
第一圖



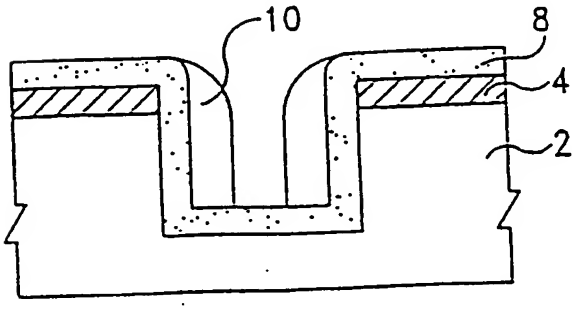
第二圖



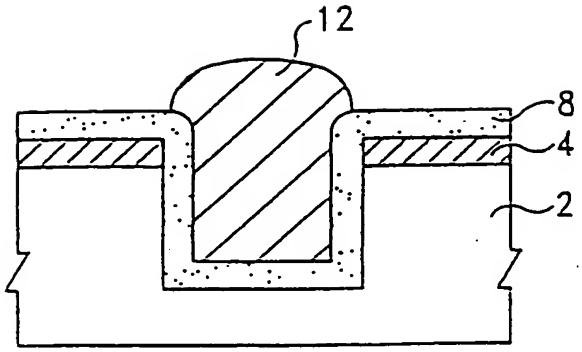
第三圖



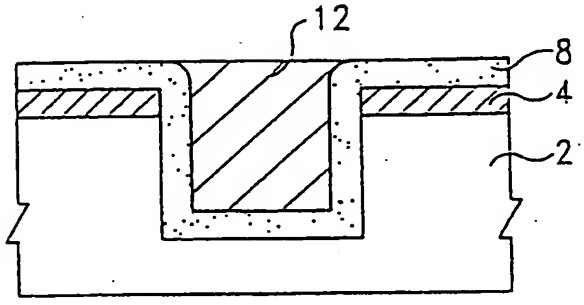
第四圖 A



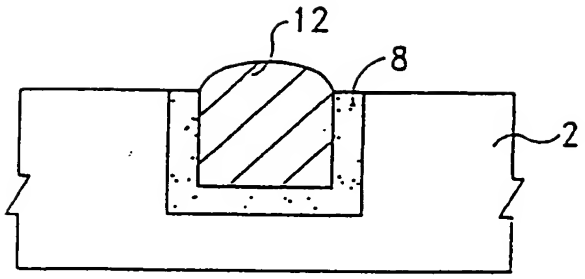
第四圖 B



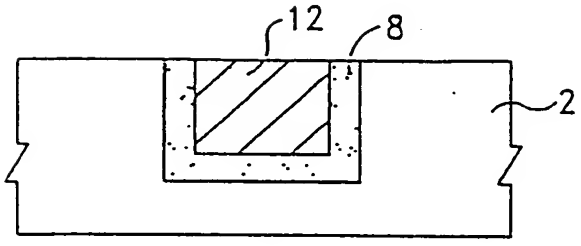
第五圖 A



第五圖 B



第六圖 A



第六圖 B

93. 2. 13

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正本

經濟部智慧財產局專利核駁審定書

受文者：爾必達存儲器股份有限公司（代理人：周良謀 先生、周良吉 先生）

地　　址：新竹市東大路一段一一八號十樓

發文日期：中華民國九十三年二月十一日

發文字號：（九三）智專二（一）04079字第〇九三二〇一二三一〇〇號

一、申請案號數：〇九一一二二六九二　　專利分類IPC(7)…H01L 21/76

二、發明名稱：使用淺渠溝隔離之半導體裝置與其製造方法

三、申請人：

名稱：爾必達存儲器股份有限公司

地址：日本

四、專利代理人：

姓名：周良謀 先生

地址：新竹市東大路一段一一八號十樓

姓名：周良吉 先生

地址：新竹市東大路一段一一八號十樓

五、申請日期：九十一年十月一日

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09320123100

六、優先權項目：

1 2001/10/09 日本2001-312034

七、審查人員姓名：賴炳昆　委員

八、審定內容：

主文：本案應不予專利。

依據：專利法第二十條第二項。

理由：

（一）所請「使用淺渠溝隔離之半導體裝置與其製造方法」其主要技術特徵為：淺渠溝內包含一底部厚度較側壁為薄(或僅留側壁)之可釋放基板內應力之絕緣層(氮化矽或氮氧化矽)。又可在該絕緣層與基板間形成一氧化矽膜。

（二）經查2001年8月21日公告之US6277706號案「METHOD OF MANUFACTURING ISOLATION TRENCHES USING SILICON NITRIDE LINER」(如引證附件一，其日本相對應公開案：特開平11-3936，併如引證附件二)，即已揭示與本案相同之技術構思：在淺溝渠內襯氧化層上以沈積一LPCVD氮化矽層，然後以蝕刻方式保留淺溝渠側壁氮化矽層(如第2(b)及2(c)圖所示)。該引證案一說明書第4欄第56至58行，尚揭示蝕刻後之氮化矽可減低作用於該氮化矽層上的應力。相較上述引證資料，本案雖在淺溝渠內氮化矽層底部之有無有，與有否具襯氧化層等技術許些差異，惟此種介電層蝕刻後殘留厚度之變化，係熟習該項

技術者可由控制蝕刻時間長暫而能輕易完成者；又本案所請在淺溝渠內襯氧化層之有無，亦是熟習該項技術者可視需要而可思及之變化，或如1998年7月11日公告之TW336344號案「溝渠式隔離區以及其形成之方法」（如引證附件三）說明書第6頁末行至次頁第2行，以及第7頁第7至9行所敘（如螢光筆劃記處）。故本案所請不具進步性。

（三）綜上所述，本案係運用申請前既有之技術或知識，而為熟習該項技術者所能輕易完成者，難謂符合發明專利要件。

據上論結，本案不符法定專利要件，爰依專利法第二十條第二項，審定如主文。

局長 蔡練生

依照分層負責規定授權單位主管決行

如不服本審定，得於文到之次日起三十日內，備具再審查理由書一式二份及規費新台幣陸仟元整（專利說明書及圖式合計在五十頁以上者，每五十頁加收新台幣五百元，其不足五十頁者以

五十頁計），向本局申請再審查。

訂

線